

# A Multi-Functional Reconfigurable Metasurface: Electromagnetic Design Accounting for Fabrication Aspects

Alexandros Ptilakis<sup>ID</sup>, Odysseas Tsilipakos<sup>ID</sup>, *Senior Member, IEEE*, Fu Liu<sup>ID</sup>, *Member, IEEE*, Kypros M. Kossifos<sup>ID</sup>, *Member, IEEE*, Anna C. Tasolamprou<sup>ID</sup>, Do-Hoon Kwon<sup>ID</sup>, *Senior Member, IEEE*, Mohammad Sajjad Mirmoosa<sup>ID</sup>, *Member, IEEE*, Dionysios Manassis, Nikolaos V. Kantartzis<sup>ID</sup>, *Senior Member, IEEE*, Christos Liaskos<sup>ID</sup>, *Member, IEEE*, Marco A. Antoniadis<sup>ID</sup>, *Senior Member, IEEE*, Julius Georgiou<sup>ID</sup>, *Senior Member, IEEE*, Costas M. Soukoulis, Maria Kafesaki<sup>ID</sup>, and Sergei A. Tretyakov<sup>ID</sup>, *Fellow, IEEE*

**Abstract**—In this article, we present the theoretical considerations and the design evolution of a proof-of-concept reconfigurable metasurface, primarily used as a tunable microwave absorber, but also as a wavefront manipulation and polarization conversion device in reflection. We outline the design evolution and all considerations taken into account, from the selection

of patch shape, unit cell size, and substrate to the topology of the structure that realizes the desired tunability. The presented design conforms to fabrication restrictions and is codigned to work with an integrated circuit (IC) chip for providing tunable complex loads to the metasurface, using a commercially available semiconductor process. The proposed structure can perform multiple tunable functionalities by appropriately biasing the IC. Perfect absorption for a wide range of incidence angles of both linear polarization states, accommodating a spectral range in the vicinity of 5 GHz, with potential also for wavefront control, exemplified via anomalous reflection and polarization conversion. The end vision is for such a design to be scalable and deployable as a practical HyperSurface, i.e., an intelligent multifunctional metasurface capable of concurrent reconfigurable functionalities: absorption, beam steering, polarization conversion, wavefront shaping, holography, and sensing.

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Alexandros Ptilakis and Nikolaos V. Kantartzis are with the Department of Electrical and Computer Engineering, Aristotle University of Thessaloniki, 54124 Thessaloniki, Greece, and also with the Institute of Electronic Structure and Laser, Foundation for Research and Technology Hellas, 71110 Heraklion, Greece (e-mail: alexpiti@auth.gr).

Odysseas Tsilipakos, Anna C. Tasolamprou, and Maria Kafesaki are with the Institute of Electronic Structure and Laser, Foundation for Research and Technology Hellas, 71110 Heraklion, Greece.

Fu Liu, Mohammad Sajjad Mirmoosa, and Sergei A. Tretyakov are with the Department of Electronics and Nanoengineering, Aalto University, 00076 Aalto, Finland.

Kypros M. Kossifos and Julius Georgiou are with the Department of Electrical and Computer Engineering, University of Cyprus, 1678 Nicosia, Cyprus.

Do-Hoon Kwon is with the Department of Electrical and Computer Engineering, University of Massachusetts Amherst, Amherst, MA 01003 USA.

Dionysios Manassis is with System Integration and Interconnection Technologies, Fraunhofer IZM, 13355 Berlin, Germany.

Christos Liaskos is with the Institute of Computer Science, Foundation for Research and Technology Hellas, 71110 Heraklion, Greece, and also with the Computer Science Engineering Department, University of Ioannina, 45110 Ioannina, Greece.

Marco A. Antoniadis is with the Department of Electrical and Computer Engineering, University of Cyprus, 1678 Nicosia, Cyprus, and also with the Department of Electrical, Computer and Biomedical Engineering, Ryerson University, Toronto, ON M5B 2K3, Canada.

Costas M. Soukoulis is with the Institute of Electronic Structure and Laser, Foundation for Research and Technology Hellas, 71110 Heraklion, Greece, also with the Ames Laboratory—U.S. DOE, Iowa State University, Ames, IA 50011 USA, and also with the Department of Physics and Astronomy, Iowa State University, Ames, IA 50011 USA.

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**Index Terms**—Intelligent reconfigurable metasurface, polarization control, tunable perfect absorption (PA), wavefront manipulation.

## I. INTRODUCTION

RECONFIGURABLE metasurfaces are electromagnetically ultrathin sheets, which are able to deploy tunable electromagnetic (EM) functions on demand. They consist of subwavelength elementary units, the meta-atoms, which can be engineered to enable interactions between the metasurface and the incoming wave [1]–[4]. This meta-atomic-level manipulation has opened a path to the realization of a plethora of EM functions and applications involving wavefront shaping [5]–[10], polarization control [11]–[13], dispersion engineering [14], [15], perfect, broadband and asymmetric absorption [16]–[20], holography [21], imaging [22], non-reciprocity [23], extreme energy accumulation [24], wireless power transfer [25], harmonic generation [26], and so on. The key element in a reconfigurable metasurface is to have an inclusion (material or component) whose EM properties can be modified by an external stimulus. Following this rationale, various tunable EM functions have been demonstrated in metasurfaces that comprise stimulus-sensitive materials, such as graphene [27], [28], liquid crystals [29], and

photoconductive semiconductors [30]. In the communications community, the use of tunable metasurfaces, also referred to as reconfigurable intelligent surfaces (RIS), for control and optimization of the wireless propagation environment is actively discussed [31], [32].

Most of the initial implementations referred to globally tunable metasurfaces, imposing limitations related to the lack of local control over the metasurface impedance. Clearly, for a multifunctional reconfigurable metasurface, an independently varying element is required in each unit cell to enable local control and reconfigurability. A practical solution to this problem, highly suited to microwave realizations, is given by incorporating lumped electronic elements in the meta-atoms. In this way, the local impedance of the metasurface can be modified by applying dc voltage signals (biasing) at the elements, which are typically p-i-n switch diodes and p-n varactor diodes. Switch diodes have been widely used in global or local binary-state scenarios for functional metasurfaces [21], [33]–[39]. However, binary-state control still restricts the realizable functions as the impedance configurations along the metasurface are limited. Varactor diodes, on the other hand, provide continuous but mainly reactive control and, thus, the ability to tune only the imaginary part of the surface impedance.

In [40], we presented a model metasurface with conceptual tunable integrated circuits (ICs) incorporated in each unit cell to allow for full control over the complex surface impedance, i.e., independently and continuously variable resistance and capacitance. This full impedance control enables one to spatially shape both the phase and amplitude of the local reflection (or transmission) coefficient and allows maximum versatility in the realizable functionalities. More importantly, this concept can infuse “intelligence” in a metasurface programmatically controlled by a computer, the so-called HyperSurface (HSF). In addition, by interconnecting more advanced ICs (with more functions such as sensing the current besides providing the tunable loads) in all the unit cells, forming a network, the vision of an intelligent metasurface fabric can be realized, where each unit can sense the ambient conditions through the powerful IC, communicate information within the metasurface and with the main controller (computer), and perform its own programmable computing and actuation, with many applications within the emerging “Internet-of-Things” paradigm [41]–[47].

In this article, we address the problem of designing a practical, multifunctional and reconfigurable metasurface for operation at microwave frequencies (5 GHz), taking fabrication constraints into account. We show, for the first time, control over the amplitude, wavefront, and polarization of the output wave in a single reconfigurable hardware platform. The metasurface consists of square patches placed on a metal-backed dielectric layer. It includes an envisaged custom IC (or “chip”), strategically placed behind the metal backplane, allowing to impose independent complex loads to each patch. We thoroughly present the design process of the multifunctional reconfigurable metasurface, from the perspective of the EM considerations and the implementation restrictions of the envisaged IC. We then evaluate the performance

of the metasurface as a tunable perfect absorber, which is the primarily targeted functionality, and show successful operation at the design frequency for a range of incidence angles of both TE and TM polarizations. In addition, we demonstrate its potential for wavefront manipulation functionality, exemplified through anomalous reflection and polarization control capabilities, showcasing the multifunctional nature of the proposed system and its control over the amplitude, wavefront, and polarization properties of the output EM wave. Control over the frequency content of the impinging radiation could also be possible with the proposed linear metasurface, by using fast time modulation of the loads provided by the ICs. Additional steps toward the realization of this metasurface with a prime focus on the custom ICs implementation and practical aspects of the printed circuit board (PCB) design can be found in [48].

This article is organized as follows. In Section II, we present the evolution of the metasurface unit-cell design from the simple proof-of-concept version to a practically feasible prototype; dedicated subsections address different design aspects pertaining to metasurface topology and operation, basic structural decisions, available range from the custom IC, fabrication and practical restrictions, and, finally, the simulation design strategy we have followed, relying on S-parameters of both lumped and Floquet ports. In Section III, we present the final design of the unit cell of the tunable perfect absorber metasurface, backed by full-wave simulation results for performance evaluation and parameter sensitivity. In addition, we assess the performance for indicative beam steering and polarization conversion functionalities. Finally, Section IV provides a summary and discusses future prospects and open challenges of such reconfigurable metasurface applications.

## II. CONCEPTUAL DESIGN AND PRACTICAL CONSIDERATIONS

EM design of a locally tunable multifunctional metasurface, which can be readily manufactured with existing fabrication processes and at a reasonable cost, poses practical challenges that can only be met with multifacet considerations and performance compromises. This section addresses the design considerations needed to select and develop the most appropriate topology, allowing as general reconfigurability as possible and leading to a realistic metasurface design. We consider both EM response and practical considerations, as well as simulated dynamic load tunability of the IC, while accommodating for the broadest possible functionalities. Readers familiar with unit-cell design methodology can skip this section and jump to the final design and performance results in Section III.

### A. EM Considerations for the Design of Versatile and Fully Reconfigurable Metasurfaces

Probably, the most natural choice for a topology of a tunable metasurface for microwave applications is the classical high-impedance surface formed by a subwavelength array of metal patches over a grounded dielectric layer [49]–[51]. The patches can be either connected to the ground by metal vias (the so-called “mushroom” structure [49]) or left floating

[52], [53]. The vias pins affect the oblique-incidence performance for TM-polarized excitation [54], [55]. This structure allows control over both amplitude and phase of the reflection coefficient by controlling the patch array only. It is very simple and compact and can be manufactured using conventional PCB technologies.

1) *Uniform Distribution of Control Elements Versus Clustering*: The simplest way to tune the metasurface response is to modify the gap capacitance between the patches, using both varactors [33], [35], [50], [51], [56], [57] and MEMS capacitors [58]. For plane-wave illumination, the response of the metasurface is determined by the parallel-type resonance of the distributed capacitance of the patch array and the inductance due to the magnetic flux between the ground plane and the patch array [52]. Thus, it appears reasonable to connect tuning elements (most commonly, varactors) into every gap between metal patches, and this topology was indeed used in [33], [35], [50], [51], [56], [58], and other works.

This approach works well for surface-uniform biasing or for slowly varying biasing (tunable phase-gradient metasurfaces). However, there are applications where fast (on the wavelength scale) tunable variations of the surface properties are needed. For example, to realize anomalous reflection from normal incidence to near-grazing direction, the so-called metagratings [59]–[61] offer arguably the most reasonable solution. To realize this regime, we need to configure the metasurface as a periodical array of electrically small elements with the period of the order of the wavelength. Moreover, to enable anomalous reflection into arbitrary directions, we need to have a possibility to configure the metasurface as a nonlocal, inhomogenizable periodical array (with the period from  $1.5\lambda$  to  $3\lambda$ ) where each supercell contains several small elements, all of them being different [62]. The conventional topologies of tuning the surface-averaged sheet reactance of the patch array are not optimal for realization of these more demanding functionalities because the change of each control element strongly affects the collective response of the whole array of patches [62].

For this reason, it appears preferable to form the metasurface as an array of patch clusters with independent control. The simplest topology of a cluster consists of four patches with control units between them, as shown in Fig. 1(a). In this topology, the patches of the two neighboring clusters are coupled only through the gap capacitance, while in the usual, uniform layout, there is also the admittance of the control unit. Such a cluster can be viewed as one patch with tunable anisotropic sheet impedance. Setting several clusters in the same or similar states, it is possible to tune the surface-averaged sheet impedance and realize phase-gradient metasurfaces or tunable absorbers. In the other extreme scenario, it is possible to connect four patches of one unit cell to the ground by different impedances, realizing one electrically small unit cell behaving as a tunable bianisotropic scatterer, whereas other clusters are tuned away from the resonance. In this way, it is possible to realize tunable diffraction gratings (metagratings [59]). Finally, we note that the control elements can be active or time-varying, opening possibilities to create amplifying, non-Foster, and nonreciprocal reconfigurable metasurfaces.

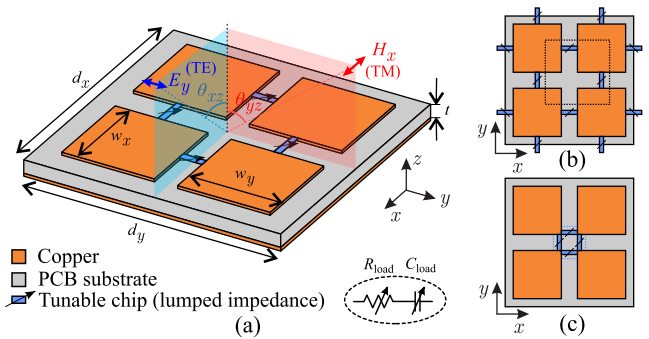


Fig. 1. (a) Extension of the proof-of-concept  $1 \times 2$ -patch unit cell to an isotropic  $2 \times 2$  cell. The new cell comprises four square patches on a thin metal-backed dielectric substrate. Its response is controlled by the ICs, modeled as complex lumped loads connecting each pair of patches. Variants of the isotropic unit cell with (b) two ICs and halved width, as denoted by the dotted-line rectangle, and (c) a single IC incorporating all four connections, in the middle of a full-width cell.

The cluster layout provides the most general reconfigurability. Note that this patch layout is similar to that used in [57], where only uniform bias has been considered.

2) *Optimal Patch Shape*: Next, we explain the reasons for selecting the square metal patches for varactor-tunable metasurfaces. In the literature on high-impedance surfaces and artificial magnetic conductors, one can find suggestions of using patches of many different shapes, from simple Jerusalem crosses and various spiral shapes to space-filling curves (see [63]–[65]). Shapes other than simple squares are used when there is a need to reduce the thickness of the structure and/or the size of the unit cell. In all these solutions, the equivalent circuit of the patch array contains an additional inductance. This inductance increases the total inductance of the parallel resonant circuit (the main inductance is due to the magnetic flux between the patch array and the ground plane), bringing the resonant frequency down and allowing reduction of the substrate thickness. However, this additional inductance reduces the bandwidth of the resonator because it is in series with the capacitive branch [51], [66]. Thus, if there is no need for reduction of the substrate thickness, it is clearly preferable to choose square patches with small gaps. If there is a need for miniaturization, it is preferable to increase the effective capacitance of the patch array by using double layers of patches instead of replacing wide patches by thinner strips of any shape.

Another related issue is the isotropy of the surface. For most applications, it is desirable that the properties of the metasurface are isotropic in the metasurface plane. In this respect, the use of hexagonal patches is preferable since the anisotropy of such arrays (assuming the same patch area) is considerably weaker than the square patch array. However, this difference can be usually neglected for small array periods, and the square shape is still preferable due to a reduced number of control elements; in this work, we adopt the square topology for the structure.

3) *Optimal Unit-Cell Size*: In practice, it is desirable to use the smallest possible number of tunable unit cells to minimize complexity and costs. This means that we should select the largest size of the unit cell, still allowing the target functions.

If the target functionality is to control the reflection for plane-wave illuminations (e.g., tunable absorbers for varying frequency, incidence angle, and polarization), there is no need for control of the surface properties at the subwavelength scale. A periodical array with period smaller or equal to  $\lambda/2$  will not create grating lobes, and we can configure all the unit cells identically, realizing an effectively uniform lossy boundary, matched to free space for the desired frequency, incidence angle, and polarization. Thus, for this application, the optimal unit cell size equals  $\lambda/2$  at the highest operational frequency.

Another important functionality is anomalous reflection with moderate deflection angles. In this case, the array should be configured as a phase-gradient metasurface, which is the conventional phased-array antenna (reflectarray) [67]. As is well known, also, in this case, the use of  $\lambda/2$ -size array elements is appropriate. However, in this case, the array is not uniform, and there is some scattering into parasitic propagating Floquet modes. Reducing the unit-cell size makes the effective (surface-averaged) response more uniform, reduces scattering, and improves the bandwidth [67], [68]. However, improvements are not very dramatic because, for moderate deflection angles (for normal illumination, up to about  $30^\circ$  to  $40^\circ$ ), the parasitic scattering is small [62], with only a few percent loss in power efficiency.

More severe limitations need to be considered if the goal is to enable arbitrary shaping of reflected waves in the far field. In general, two different configurations are needed: diffraction grating (metagrating) and nonlocal metasurfaces. In the first case, the period is of the order of the wavelength and we need to “activate” only one or two elements, whereas the rest are set far from the resonance. In the second case, the period is larger than  $\lambda$  but still comparable to it. As demonstrated in [62], in this case, we need about 8 to 10 unit cells per period, and all the cells are in general configured differently to enable efficient anomalous reflection to large angles. To enable both these regimes, it is appropriate to select the unit-cell size not larger than about  $\lambda/5$ . Together with the clustering discussed earlier, selection of this size enables the most general reconfigurability of metasurface reflectors.

4) *Choice of the Substrate Permittivity and Thickness:* As is well known from the theory of high-impedance surfaces, higher permittivity improves the stability of the resonant frequency with respect to the incidence angle and allows reduction of the substrate thickness but decreases the bandwidth [66]. For reconfigurable surfaces, the angular response can be adjusted by tuning the unit cells, whereas wider frequency bandwidth is desirable for robust operation. In addition, there is also the practical consideration of availability of cheap and fabrication-friendly low-loss substrates. In view of these considerations, we select moderate-permittivity low-loss dielectric substrates. The thickness of the substrate mainly determines the effective inductance of the equivalent parallel resonant circuit, which models the high-impedance circuit [49], [52]. Higher inductance means higher bandwidth, meaning that thicker substrates are preferable. Naturally, the thickness should be still considerably smaller than the wavelength.

5) *Proof-of-Concept Study:* These general design considerations have been recently validated for plane-wave illuminations in two orthogonal planes, parallel to the principal axes of an array of square patches [40]. The unit cell of this metasurface is schematically shown in Fig. 1(a). In these illumination scenarios, it is enough to consider only pairs of loaded square patches because there is no current over the other two loads. The load impedance was assumed to be complex, with variable capacitance and resistance. The studied range of capacitance variations was 1 to 5 pF, corresponding to the parameters of commercially available chip varactors for the target frequency range (about 5 GHz) and similar to the ranges of varactors used in recent experimental studies of tunable high-impedance surfaces [56], [57]. The tunable resistance was assumed to be varying from 0 to 5  $\Omega$ , again in harmony with the parameters of commercial chip varistors, and allowing comparison with ideal, lossless structures.

The most critical issue was to validate the hypothesis that it is possible to realize near-perfect anomalous reflectors, not limited to any angular sectors, by tuning only load reactances of unit cells, while their sizes and shapes remain fixed and the same for all cells. The only known earlier realization of this functionality relied on careful optimization of sizes of subwavelength patches forming supercells of a periodical lattice [62]. The results presented in [40] have shown that comparable performance can also be achieved using the proposed topology of fixed-size arrays of patch clusters with variable reactive loads, with practically realistic values of load capacitances. The study of tunable absorber configurations has shown that the same metasurface can be indeed configured to the regime of full absorption of incident plane waves of both TE and TM polarizations, as shown in Fig. 1(a), in a wide range of incidence angles.

### B. From the Proof-of-Concept Unit Cell to Fully Reconfigurable Implementable Unit Cell Design

For practical implementation, we start from the structure in [40], which is only a proof-of-concept design and there is still a long way toward industrial realization. For example, some open questions include the following. How should the chip be connected to the patches and how would the connectors affect the performance of the metasurface? Is the design compatible with fabrication technologies? How can the capacitive and resistive loads be optimally realized in practice? In this and in the following, we discuss all these practical issues and, based on these considerations, we propose a practically realizable reconfigurable metasurface.

1) *One Chip Instead of Four Chips per Cluster:* The cluster topology shown in Fig. 1(a), with four chips connecting the patches, is not cost-effective or practical to populate. In addition, more complex routing lines are required when communications between the chips are demanded for programmability. Moreover, when the unit cell size is in the 10 mm order ( $\lambda/6$  at 5 GHz), squeezing four chips inside such a small area demands advanced fabrication technologies, which again raise the cost. A simple and effective solution is to use just one chip inside each unit cell, as shown in Fig. 1(c).

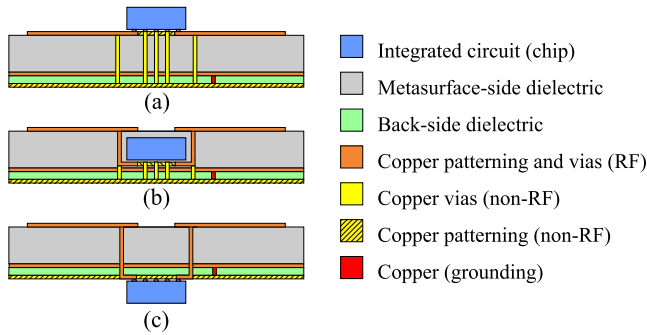


Fig. 2. Investigating the optimal vertical position of the chip, with respect to the number of vias and metallization layers required. Vertical cross sections of possible designs where the chip is (a) on the top layer, (b) embedded inside the dielectric, and (c) behind the backplane.

To enable the same functionalities, one chip is now essentially supporting at least four  $RC$  pairs. With this simplification and the change of the  $RC$  connection from the middle of the patch edge to the patch corner, the metasurface can still support the desired functionalities. In addition, we note that in this way, we also select the best position for the load connection, i.e., the patch corner, because that is where the surface charge density maximum across the patch is located for illumination in both primary incidence planes of the structure shown in Fig. 1(a).

2) *Load Connection Topology Inside the Chip*: Another issue raised in the “one chip per cell” approach is the choice of the patch-load-patch connecting topology, as well as the number of loads inside the chip. For practical reasons related to unavoidable parasitics inside the chip, as detailed in [48], an X-shaped connection was finally adopted with four independent loads connecting the corner of each patch to the common ground pin in the center of the chip. This load topology can readily implement the absorber functionality by setting all loads to the same  $RC$  values and can also accommodate other functionalities, e.g., anomalous reflection and polarization conversion (with different  $RC$  values).

3) *Out-of-Plane Chip Placement*: A key decision that should be made is the placement of the chip in the vertical sense. Three options were examined: 1) on the top patch layer; 2) embedded inside the substrate, and 3) below the ground plane, as schematically shown in Fig. 2. Option 1) was abandoned because the chip would interfere with the incident radiation thus disrupting the performance; in addition, a large number of through vias (TVs) together with traces and landing pads (as TVs cannot be fabricated directly below the chip) would be required to pass communication and powering lines behind the backplane, and these vias/traces/pads would complicate and degrade the EM response, especially for TM polarization. Option 2) was also abandoned because embedding the chips involves costly nonstandard fabrication processes; moreover, it excludes probing and servicing malfunctioning chips postfabrication and also requires a large number of blind vias. The optimal option for chip placement is behind the backplane, with only four TVs penetrating it to connect to the back side of each patch, as shown in Fig. 2(c). From the EM design point of view, option 3) ensures that all the

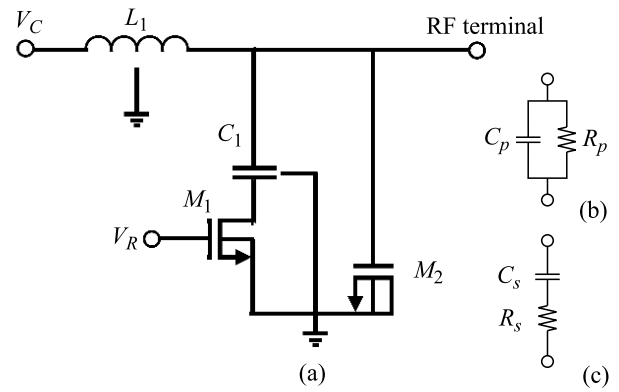


Fig. 3. (a) Simplified metasurface loading element circuit. Equivalent (b) parallel and (c) series  $RC$  circuit representation of the metasurface loading element between the ground and the RF terminal/port.

auxiliary chip wiring does not affect wave propagation, while the metasurface properties can be reconfigured.

Finally, a last issue is the position of the four TVs connecting the chip RF terminals to the patches. While, in mushroom structures, the vias are located at the center of the patches, here, we stress that for a reconfigurable metasurface, the optimal position for vias is at the patch corner closest to the chip. That is where the surface current density is at its maximum for illumination in both primary incidence planes, and therefore, the impedance introduced by the chip can more widely control the metasurface response.

### C. IC Design

In this section, the custom IC design of the metasurface loading elements ( $R$  and  $C$ ) is presented. The architecture of the ICs that enable the independent control of the four complex loads was presented in [48], and it consists of an asynchronous circuit controller [45], eight digital-to-analog (D/A) converters, and four loading elements. The IC chip aims to satisfy metasurface performance, cost, and power constraints. It utilizes MOSFETs to implement both the variable capacitance (varactor)  $C$  and variable resistance (varistor)  $R$ . A simplified circuit of the metasurface loading element is shown in Fig. 3(a). In this schematic, the varistor  $M_1$  is adjusted through a gate voltage  $V_R$  (biasing voltage) and the varactor  $M_2$  is adjusted through biasing voltage  $V_C$ . The RF-choke inductor  $L_1$  is used to block the RF signal from shorting on the low-impedance node  $V_C$ . Similarly, the dc-block capacitor  $C_1$  is used to ensure the  $V_C$  voltage shorting to ground through  $M_1$ . The circuit forms a parallel connection  $RC$  load, which, at its steady state, will draw negligible current due to gate leakage. The design methodology for the lumped elements and all the actual on-chip circuit implementations of all the custom IC components (varistor, varactor, RF-choke inductor, and dc-block capacitor) can be found in [48] and references therein. We stress, once more, that our design relies on a custom IC to implement the varistor and varactor functionality and not on discrete commercially available surface-mount devices.

In the remainder of this work, we only consider the complex impedance values that are supplied by the custom IC to load

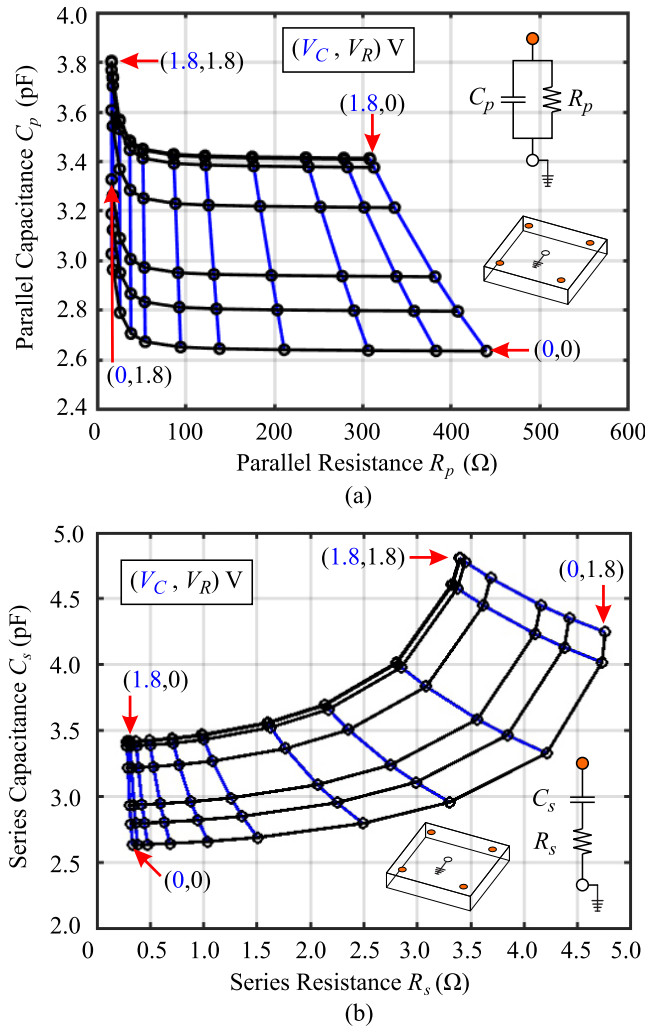


Fig. 4. Equivalent resistance and capacitance range for (a) parallel and (b) series representation at 5 GHz. The corresponding varistor and varactor voltage pairs are also annotated. In the insets, the orange-filled and empty dots represent the RF terminal and the ground of Fig. 3, respectively.

the metasurface patches. The available complex impedance range, in terms of  $RC$  values, is shown in Fig. 4, and was obtained by schematic simulations in Cadence Virtuoso. A 180 nm technology process design kit was used in the S-parameter simulation. The obtained S-parameters were converted into Z-parameters and in turn converted into an equivalent parallel or series  $RC$  load, as shown in Fig. 3(b) or (c), respectively. In the Cadence simulations, the supplied voltages  $V_R$  and  $V_C$  are gradually increased from zero to IC's supply voltage (1.8 V). Each combination of  $V_R$  and  $V_C$  voltages corresponds to an implemented  $RC$  value; the limit  $RC$  values, for the corresponding limit  $(V_C, V_R)$  pairs, are shown in Fig. 4 with red arrows. This defines an area with the achievable  $RC$  values of the metasurface loading element. The values can be converted from parallel to series connection, and vice versa, using the following formulas:

$$R_s = R_p(1 + Q^2)^{-1}, \quad (1a)$$

$$C_s = C_p(1 + Q^2), \quad (1b)$$

where  $Q = \omega R_p C_p = 1/\omega R_s C_s$  is the quality factor of the circuit. In the remainder of the text, we will use the equivalent series  $RC$  representation, unless otherwise mentioned.

#### D. Fabrication and Practical Restrictions Related to EM Operation

Having outlined the basic considerations that have led us to the approximate dimensioning of the metasurface unit cell in the lateral (cell and patch widths) and vertical (dielectric thickness) directions, and implementation rules for the custom IC, additional manufacturing limitations have been considered in the design.

An important design aspect is manufacturability of the TVs that will connect the IC RF terminals (on the back side of the metasurface) to the patches (on the front side of the metasurface). The available technology for TVs requires for a maximum 1:8 aspect ratio, i.e., the thickness of the material stack for the mechanical drilling of TVs must not exceed eight times the diameter of the via, so as to achieve sufficient copper via electroplating. In contrast, blind vias (BV) require a 1:1 aspect ratio, leading to relatively thicker cylinders. Simulations and fabrication concerns have recommended an approximate thickness of the dielectric stack penetrated by the TVs to be 2.4 mm, and therefore, a TV diameter of 0.3 mm was chosen. It was numerically verified that increasing the diameter of the TVs leads to a small increase in the resonance frequency, without degrading its quality factor (the amplitude of the reflection coefficient remains  $-30$  dB or lower). For example, for a TV diameter increase from 270 to 300  $\mu\text{m}$ , the resonance frequency increases by roughly 70 MHz, which can be compensated by slightly increasing the capacitance introduced at the chip terminals, well within the tuning capabilities of the chip. Finally, it should be noted that all vias are copper electroplated so that they are essentially hollow metallic cylinders, inset of Fig. 5(a); although our EM simulations were conducted assuming solid-copper vias, for the sake of simplicity, additional numerical simulations have confirmed that the two models are equivalent due to the small skin depth ( $\sim 1 \mu\text{m}$  at 5 GHz).

The next practical considerations concerned the dielectric material choices to be used above and below the metal backplane. Initial fabricated prototypes used high-frequency graded Rogers RT/duroid 5880 dielectric ( $\epsilon_r = 2.20$  and  $\tan \delta = 0.0009$ ) on the top side and regular FR4 dielectric (Hitachi MCL-E-679FGB) on the back side, where low loss is not as important to minimize cost. Fabrication of the initial three-layer substrates, e.g., as in Fig. 2(c), resulted in significant warping (bending) of the PCB after lamination of all build-up layers, even for small metasurface substrates, e.g., 10 cm  $\times$  10 cm, due to mismatch of the thermal-expansion coefficients of the two dissimilar dielectrics. For this reason, the subsequent designs used the same dielectric substrate type, namely, Panasonic Megtron7N dielectric ( $\epsilon_r = 3.35$  and  $\tan \delta = 0.0020$ ), with laminates and prepreg layers symmetrically positioned above and below the backplane, thus minimizing warping. Given the fixed dielectric thicknesses available, a stack of Megtron7N laminates and prepregs has

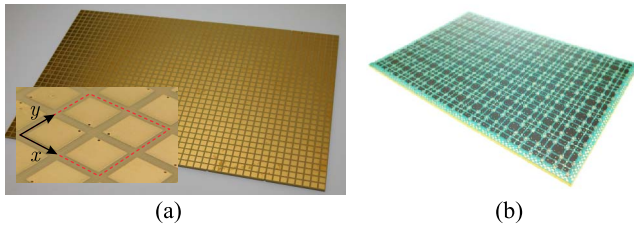


Fig. 5. Photographs of the fabricated metasurface PCB, with a net area of  $6.2 \text{ in} \times 9.4 \text{ in}$  corresponding to  $24 \times 16 = 384$  unit cells. (a) Perspective view of the front side/top layer with Ni/Au metallization. Inset: close-up view of the unit cell where the four electroplated (hollow) TVs can be seen. (b) Perspective view of the bottom side, where the custom ICs will be assembled.

been symmetrically laid up to achieve the total thickness required and ensure that warpage has been diminished; indeed, the homogeneous nature of prepregs and laminates used has yielded minimum warpage. Fig. 5 shows a view of the demonstrator metasurface substrate made of Megtron7N PCB materials for the abovementioned studies. It has been 2.4 mm thick,  $160 \text{ mm} \times 240 \text{ mm}$  ( $6.2'' \times 9.4''$ ) in size and has been produced in large industrial panels of  $457 \text{ mm} \times 610 \text{ mm}$  format.

As discussed in Section II-C, the optimal position to connect each pair of patches with lumped loads is at their corners; this can be intuitively understood by the increased surface current density at such positions, which allows for wider tunability, and by the minimization of the inductance and resistance associated with short copper paths. However, in a realistic structure, the TVs that connect the patches to the IC (modeled by lumped loads) cannot be placed very close to the patch corner for two fabrication-related reasons: first, because drilling of the TVs can only take place outside the chip footprint and, second, because the landing pads for the vias (drilled from the back to the front) are two times the via diameter and, thus, cannot be placed too close to the patch edge. The minimum values of these two offsets were chosen as  $\delta x = 0.4 \text{ mm}$  and  $\delta y = 0.2 \text{ mm}$ , respectively, and are shown in Fig. 6. Please note that the resulting unit cell exhibits structural anisotropy, enforcing only mirror symmetry and not fourfold rotational symmetry, meaning that the metasurface will behave differently for the two normally impinging polarizations ( $x$ - and  $y$ -polarized). This compromise arose from limitations stemming from the  $RC$  values due to the physics of real chips and the size of the patches and will be discussed in detail in Section III.

Concluding this part with restrictions related to the fabrication, first, it was verified that laterally offsetting the BV connecting the ground pin of the chip (which is the one in its middle) to the metasurface ground plane has no effect on the TE polarized absorber performance, our main target. Therefore, in the simulations performed in this work, a single BV was placed in the center of the chip footprint. However, in the fabricated device [48], a copper trace brings this pin outside the chip footprint where the BV will short it to the metasurface ground plane so that the chip terminals and the patches have a common reference ground. The length and path of this BV trace are expected to influence the oblique TM performance due to mutual coupling with the RF terminal traces

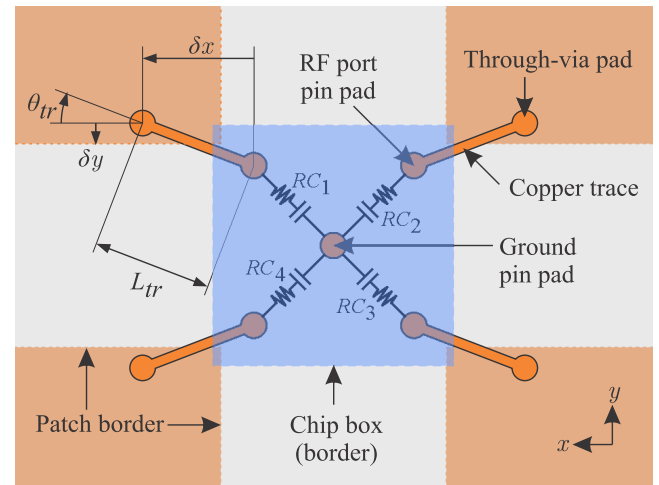


Fig. 6. View of the back side of the unit cell, depicting the lateral offsets of the TV placement imposed by fabrication limitations. Parameters  $\delta x$  and  $\delta y$  denote the minimum lateral distance of the TV pad to the corner chip-pin pad and to the inner edge of the patch, respectively. The four lumped  $RC$  elements that load the patches through the TVs can be independently controlled.

because of the current flowing through the BV (which is zero for TE polarization). Finally, in order to model the device as thoroughly as possible, one would need to quantify the effect of the solder balls used to electrically connect the RF terminals of the chip to their respective pads on the metallization layer.

### E. S-Parameter Modeling and Simulation

In order to efficiently model and simulate this multi-parametric EM problem, we rely on S-parameters, enabled by the metallic backplane, which effectively decouples the metasurface- and the chip-side designs. Thus, using the backplane as a common reference ground, we can model the chip with four lumped ports [see Fig. 7(a)] and the incident and scattered plane waves with Floquet ports [see Fig. 7(b)]. The lumped ports are  $50 \Omega$  referenced and fed by Touchstone data (complex spectra) depending on the IC architecture, i.e., ranging from a single generalized four-port network (most complicated case) to four identical decoupled  $RC$  loads (simplest case). The Floquet ports are defined for a given plane-wave direction, i.e., a  $(\theta, \phi)$  pair for incoming waves, for both polarizations (TE/TM), and are placed at the front and back side of the unit cell, at planes perpendicular to the  $z$ -axis; periodic Bloch–Floquet conditions are applied to the remaining four boundaries enclosing the unit cell, emulating infinite periodicity. Please note that in the case of uniformly configured chips we use a total of four Floquet ports; as the unit cell is subwavelength, only the zero-order (specular) diffraction order is propagating, but we generally need to consider both linear orthogonal polarizations at both sides. In the case of inhomogeneous unit cell arrangement, where a supercell with periodicity exceeding the free-space wavelength is formed, such as the anomalous reflection scenario in Section III-B, the number of Floquet ports increases to accommodate other propagating diffraction orders.

For the perfect absorber functionality, all unit cells of the metasurface must be identically configured; also, for our

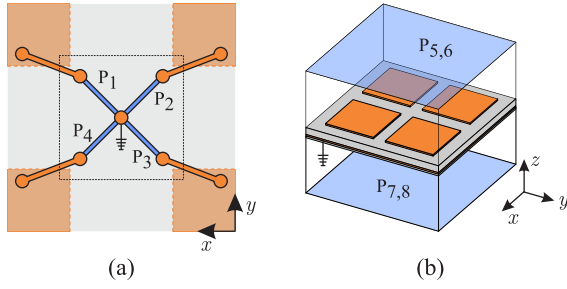


Fig. 7. Modeling of the unit cell using combination of lumped and Floquet S-parameter ports. (a) Back side of the unit cell where the four lumped ports,  $P_{1,2,3,4}$ , represents the RF ports (terminals) of the IC, individually addressed similar to the  $RC_{1,2,3,4}$  of Fig. 6. (b) Perspective view of a subwavelength unit cell depicting the four Floquet ports,  $P_{5,6}$  corresponding to TE and TM polarized ports on the front (top) side, and  $P_{7,8}$  similarly on the back (bottom) side. Floquet ports are defined on planes perpendicular to the  $z$ -axis and for a given incident plane-wave direction.

metal-backed weakly anisotropic structure, we can safely assume that transmission and cross-polarized reflection coefficients will be practically zero since the structural anisotropy was found too weak to induce polarization conversion. For these reasons, we model a single unit cell and seek the IC configuration that will lead to a minimization of the reflection coefficient  $|r|$  for a given polarization, i.e., minimization of the  $|S_{55}|$  or  $|S_{66}|$  scattering parameter for TE and TM incidence, respectively, using the port-number convention of Fig. 7. In the general case, the power absorption coefficient when exciting Floquet port  $i$  is  $A_i = 1 - \sum_j |S_{ji}|^2$ , where  $j$  runs through the Floquet ports (5 to 8).

As stated in Section II-D, we have intentionally designed the chip with its four RF ports decoupled so that they can be directly replaced by lumped loads, with their  $RC$  values falling inside the prescribed IC map (see Fig. 4). This allows us to rapidly find the chip configuration, in terms of  $RC$  pair, that leads to perfect absorption (PA) at a given frequency and polarization: For a given incident plane-wave direction, we numerically evaluate the eight-port S-parameters of the unit cell with full-3D EM simulation. Then, we attach a prescribed  $RC$  load to all four lumped ports (passed as one-port Touchstone data). Finally, we extract the scattered spectra at the remaining four Floquet ports, corresponding to the two polarizations (TE and TM) and the two sides of the unit cell (top/back sides, i.e., reflected/transmitted). Iterating over the  $RC$  loads using an optimizer, we can rapidly identify the optimal configuration for PA at a given frequency and polarization. We have confirmed that within the given  $RC$  range from the chip design, this method works perfectly as the load range is limited. However, note that changing a geometric/EM parameter of the structure and/or the incident plane-wave direction, e.g., for oblique-incidence absorption, requires numerical recalculation of the eight-port network S-parameters with a new full-3D EM simulation, which is computationally intensive (time consuming) due to the fine geometrical features. These simulations were conducted in CST Microwave Studio, using the 3-D frequency-domain solver with broadband sweep and the Design Studio environment for the eight-port S-parameter tasks.

### III. EM DESIGN OF THE COMPLETE UNIT CELL AND THE MULTIFUNCTION PERFORMANCE

In this section, we present the metasurface unit cell design, considering all the aspects and restrictions discussed in Section II. The prime focus is given on wide-angle tunable PA functionality by thoroughly analyzing its performance; steering and polarization conversion functionalities are also assessed. The different applications require different load settings within and between chips: 1) in PA (see Section III-A), all four loads in the unit cell are set to the same value and all unit cells are collectively tuned (uniform metasurface); 2) in anomalous reflection (see Section III-B), all four loads in the unit cell are set to the same value, but the unit cells comprising the supercell are tuned differently; 3) in polarization conversion (see Section III-C), all cells are collectively configured, but the loads in the unit cell are set to different values to break the fourfold symmetry of the unit cell. These settings apply for plane incoming/outgoing wavefronts and a planar (flat) metasurface.

#### A. Tunable PA

The main functionality implemented by our reconfigurable metasurface device is tunable PA of plane waves, which can impinge from a large cone of incidence directions and both polarizations. As discussed, for the IC-loaded unit cell to achieve PA at a given frequency, polarization, and direction of incidence, we must properly tune both the resistive and reactive (capacitive) part of the equivalent lumped loads inside the IC. Given the tuning ranges of the varistor and varactors in the chip design, Section II-C, the optimization of the free structural parameters of the unit cell design is performed. The reference optimization case is PA at 5 GHz, normal  $y$ -polarized incidence,  $R_s = 2.1 \Omega$ , and  $C_s = 3.2$  pF; these  $RC$  values lie approximately in the middle of the chip range, thus allowing maximum tunability. The free structural parameters of the design are essentially the cell and patch width,  $w_c$  and  $w_p$ , respectively, under the condition that the TVs are placed as close as possible to the inner patch corners, which is limited by the fabrication thresholds  $\delta x$  and  $\delta y$  discussed in Section II-D. In order to unveil the underlying design rules, one can parametrically calculate the reflection amplitude as a function of  $w_c$  and the newly defined filling ratio,  $\rho_f = 2w_p/w_c$ , with the results presented in Fig. 8. Full-wave EM simulations of the unit cell are employed, conducted in CST Microwave Studio, using the frequency-domain solver with tetrahedral mesh. An approximately linear trendline emerges, showing that smaller cells require proportionally larger patches to resonate for the same external load values. For our design, PA is achieved at the optimal values of  $w_c = 9$  mm and  $\rho_f = 0.77$ , i.e.,  $w_p = 3.465$  mm. For these parameter values, the length and angle of the metal traces connecting the RF terminals of the chip to the landing pads of the TVs defined in Fig. 6 are  $L_{tr} = 0.41$  mm and  $\theta_{tr} = -11.65^\circ$ , respectively. The resulting unit cell and structural dimensions are summarized in Fig. 9 in millimeters.

Having completed the selection of all the structural dimensions, the performance for PA functionality is assessed.



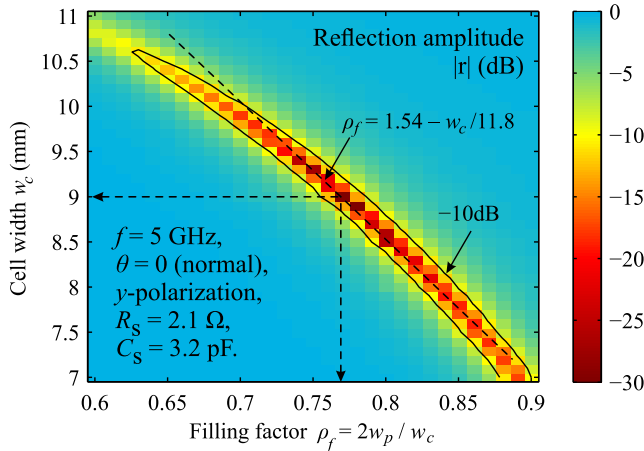


Fig. 8. Design map of the unit cell, depicting the reflection amplitude of  $y$ -polarized normally incident plane wave at 5 GHz, assuming that the chip is configured to deliver the equivalent lumped loads  $R_s = 2.1 \Omega$  and  $C_s = 3.2 \text{ pF}$  at its ports. This map allows the extraction of the optimal unit cell and patch width,  $w_c$  and  $w_p = \rho_f w_c / 2$ , respectively, with all the remaining structure parameters defined in Section II-D.

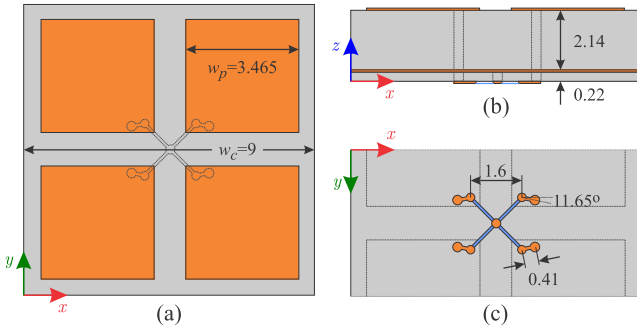


Fig. 9. Final unit-cell design and dimensions in millimeters. (a) Top view, showing the cell and patch widths. (b) Side-view cross section, showing the dielectric thickness of the top and bottom dielectrics. (c) Bottom view, showing: the X-connection shape of the four lumped ports to the ground, the locations of the TVs connecting the chip RF terminals to the patches, and the respective traces.

The amount of control imparted by resistance and capacitance tuning is shown in Fig. 10, where  $C$  and  $R$  control the resonance frequency and quality factor (resonance “depth”), respectively; these spectra are for normal  $y$ -polarized incidence. The resonance bandwidth is over 100 MHz (or 400 MHz) measured at  $-10 \text{ dB}$  (or  $-3 \text{ dB}$ ). The respective tolerance values of  $C$  and  $R$  for near PA at 5 GHz are quantified in terms of the achieved reflection amplitude,  $|r| < -10 \text{ dB}$  (see Fig. 11). The attained range falls well within the varistor and varactor range of the chip, thus allowing tuning and possible fabrication-deviation compensation.

The last step in validating the performance of the absorber is to quantify the coverage range, in terms of oblique-incidence angle and/or frequency detuning, allowed by the available  $RC$  map of the IC. The S-parameter block modeling approach described in Section II-E is employed in order to efficiently calculate the optimal load impedance values for various combinations of incidence direction, polarization, and frequency. The results are presented in Fig. 12. Oblique-incidence coverage is up to  $60^\circ$  for

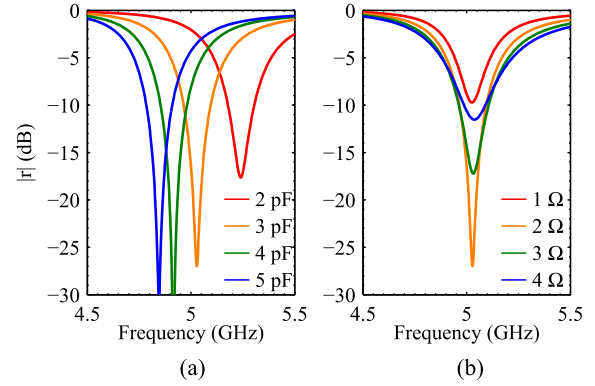


Fig. 10. Indicative spectra of the reflection amplitude for normal  $y$ -polarized incidence. (a) Series capacitance tuning affects the absorption resonance frequency for fixed  $R_s = 2 \Omega$ . (b) Series resistance tuning affects the resonance quality factor, i.e., “depth,” for fixed  $C_s = 3 \text{ pF}$ .

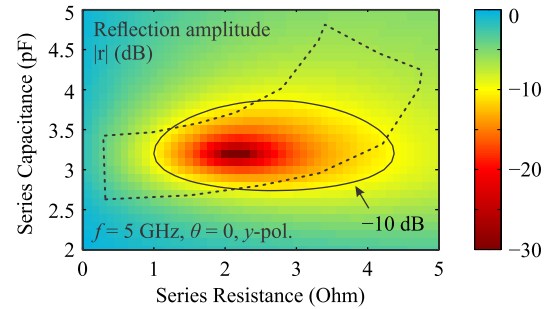


Fig. 11. Reflection amplitude for  $y$ -polarized normal incidence at 5 GHz, as a function of identical series  $RC$  loads attached to all four ports. The dotted area is the  $RC$  values allowed by the IC.

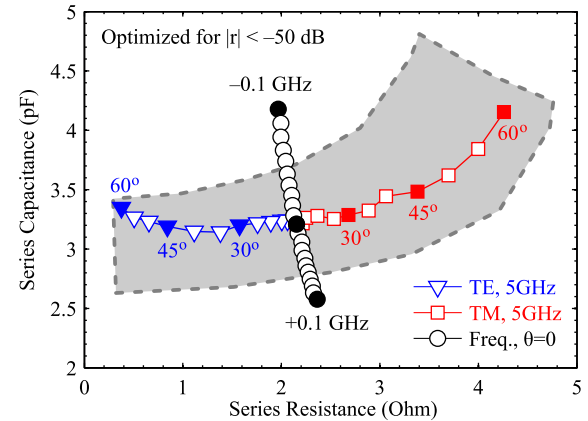


Fig. 12. Coverage for oblique incidence and frequency detuning for the tunable PA functionality of the final unit cell in terms of series  $RC$  loads. Oblique incidence is at 5 GHz with angle steps of  $5^\circ$ ; frequency detuning is in steps of 10 MHz.  $y$ -polarized incidence is assumed in all cases, i.e., the plane of incidence is  $xz$  and  $yz$  for TE and TM case, respectively.

both TE and TM polarization planes as defined in Fig. 1(a), i.e., with the electric field always primarily polarized along the  $y$ -axis, where the lateral distance between the TVs is smallest. Frequency tuning is limited to  $\pm 50 \text{ MHz}$ , due to the sharp absorption resonance and the limited capacitance range.

1) *Cross-Polarized Absorption Performance*: Since the targeted metasurface functionality was widely tunable PA for at

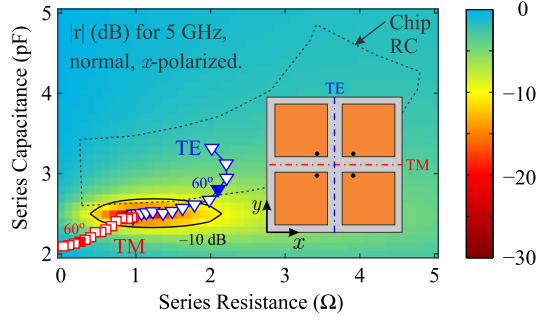


Fig. 13. Cross-polarized tunable absorption performance at 5 GHz. The colormap corresponds to reflection amplitude of  $x$ -polarized normal incidence as series  $RC$  lumped loads are varied. Optimal  $RC$  values for oblique incidence ( $5^\circ$  steps) in TE and TM planes are superimposed, with blue triangles and red squares, respectively. The inset depicts how TE and TM planes are defined in the anisotropic unit cell for the cross-polarized case.

least one polarization, the unit cell design was allowed to be anisotropic, i.e., to exhibit mirror symmetry but not fourfold rotational symmetry, as shown in Fig. 9(a). In this regard,  $y$ -polarization (i.e.,  $E_y$  in TE and  $E_{yz}$  in TM) will outperform  $x$ -polarization, for PA on the given  $RC$  range. We opted for this tradeoff, in order to have at least one of the polarizations perfectly absorbed and with wide oblique-incidence tunability; trying to accommodate both polarizations in the limited  $RC$  range while enforcing fourfold symmetry (i.e., traces angle  $\theta_{tr} = 45^\circ$  and  $L_{tr} \leq \sqrt{2}\delta x$ , as defined in Fig. 6) led to meager simulated performance for both polarizations and/or very limited oblique-incidence coverage. Nevertheless, we assessed the cross-polarized absorption performance, with the results summarized in Fig. 13. As expected, very limited coverage is offered, e.g., only highly oblique  $x$ -polarized (TE) incidence can be perfectly absorbed for the given  $RC$  coverage, while suboptimal performance, e.g., reflection as high as  $|r| \approx -10$  dB, can be attained for normal incidence.

2) *Double Resonance at Highly Oblique Incidence*: It must be noted that highly oblique-incidence cases give rise to an interesting phenomenon of dual absorption resonance. For instance, in the  $\theta = 60^\circ$  TE  $y$ -polarized case, we can clearly see two minima of reflection spaced by approximately 100 MHz [see Fig. 14(a)]. Naturally, the unit cell  $RC$  values can be tuned to optimize either of the two resonances for absorption at the desired frequency, as shown in the tolerance map of Fig. 14(b). The series resistance is approximately the same,  $0.35 \Omega$  in this case, whereas the series capacitance can vary up to 1 pF. This double resonance gradually emerges for  $\theta > 45^\circ$ , being more pronounced for  $y$ -polarized waves in the C-band (5 GHz) for our unit cell design.

### B. Anomalous Reflection

The independent control over the  $RC$  values in each unit cell enables us to perform wavefront manipulation operations, such as anomalous reflection. Although the reflection amplitude is low within the realizable  $RC$  range by the chip (see Fig. 11), the coverage of the reflection phase is quite large, i.e., from  $-170^\circ$  to  $+170^\circ$ , as shown in Fig. 15(a). As a result, anomalous reflection can be achieved if we lower the

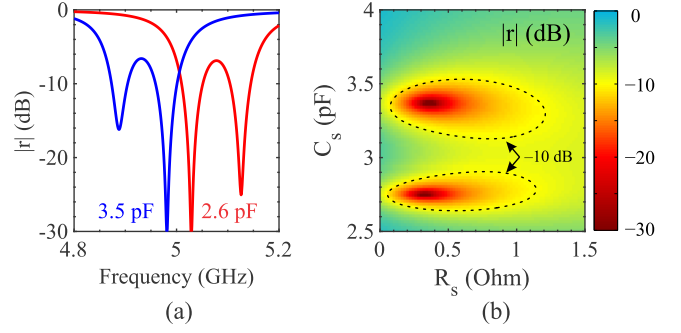


Fig. 14. Double absorption resonance arising for very oblique TE incidence angles. (a) Reflection amplitude spectra for  $\theta = 60^\circ$ ,  $y$ -polarized,  $R_s = 0.35 \Omega$ , and two different values of series capacitance  $C_s$ . (b) Reflection amplitude at 5 GHz, depicting the two optimal series- $RC$  configurations available.

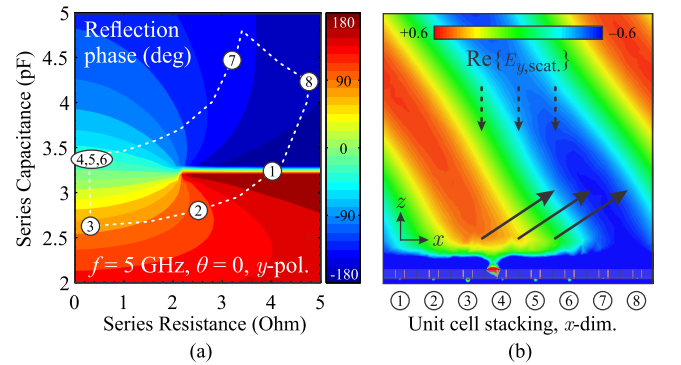


Fig. 15. (a) Reflection phase of homogeneous metasurface setting for 5 GHz, normal,  $y$ -polarized incidence; the white circles depict the series  $RC$  settings for the eight unit cells, required for anomalous reflection function. (b) Scattered  $E_y$  field pattern for anomalous reflection function.

requirement on the reflection amplitude. Anomalous reflection is obtained by grouping several unit cells into a supercell and allowing the reflection toward the desired direction while forbidding the scattering to other directions by selectively promoting a single propagating diffraction order over the others. Utilizing different supercell sizes and relying on different diffraction orders, the anomalous reflection direction can be tuned with a quasi-continuous angle coverage [40]. To demonstrate the anomalous reflection effect, we consider a supercell made of  $N = 8$  unit cells, which will support anomalous reflection from normal incidence toward the  $56.4^\circ$ , according to  $\theta_r = \arcsin(\lambda_0/D)$  [9], [40], where  $D = Nd_x$  is the extent of the supercell. In this supercell configuration, which is different from the one in Fig. 7, there are three ports,  $a$ ,  $b$ , and  $c$ , corresponding to the three propagating diffraction orders  $m = 0, +1, -1$  (since  $\lambda_0 < D < 2\lambda_0$ ). Note that transmission and polarization conversion is negligible and, thus, power collected by the corresponding ports is negligible. Subsequently, we perform an optimization while constraining the  $RC$  values within the realizable range. Note that in order to speed up the optimization process, one can use as an initial setting for the  $RC$  values those dictated by a linear phase profile along the supercell, i.e.,  $\phi(x) = \phi_0 - (2\pi/D)x$  [40].

The required  $RC$  values for the eight unit cells after optimization are shown as white dots in Fig. 15(a). With this

configuration, the normally incident wave with polarization  $E_y$  is reflected to  $56.4^\circ$  ( $m = +1$ , port  $b$ ) without prominent scattering to the specular direction ( $m = 0$ , port  $a$ ) or the  $m = -1$  diffraction order ( $-56.4^\circ$ , port  $c$ ), as verified by the scattered  $E_y$  field pattern shown in Fig. 15(b). The amplitude of the anomalous reflection coefficient is  $|S_{ba}| = 0.38$ , which means that 14.4% of the power is reflected toward the desired direction. Meanwhile, the amplitudes of the reflection coefficients to the other two directions are  $|S_{aa}| = |S_{ca}| = 0.05$ . The absorbed power by the metasurface is given by  $A_a \approx 1 - \sum_n |S_{na}|^2 = 85.1\%$ , where  $n$  runs through the propagating reflection diffraction orders  $\{a, b, c\}$ ; an anomalous reflection efficiency of  $\text{Eff}_{ba} = |S_{ba}|^2 / \sum_n |S_{na}|^2 = 96.7\%$  is calculated, meaning that 96.7% of the scattered power goes to the desired direction. The low reflection amplitude is primarily due to the custom IC imposing a limited  $RC$  tuning range and, secondarily, due to fabrication restrictions; in principle, having a broader  $RC$  range and less fabrication constraints would allow tuning the unit cell far from its absorption resonance, thus allowing much higher reflection amplitude with an ample phase span. Finally, we emphasize that through the same principle of locally modifying the reflection phase by changing the  $RC$  loads, we can achieve more wavefront manipulation operations, such as retroreflection and focusing [9], [40].

### C. Polarization Conversion

Next, we exploit additional advantages of the proposed unit cell configuration. Organizing patches in groups of four and using a single chip to control them was judiciously chosen to save resources and, in principle, to lead to a geometrically isotropic unit cell design that could have polarization-independent response. On the other hand, however, this patch connectivity offers the distinct capability of electrically breaking any rotational symmetry, thus leading to polarization conversion.

Here, as a demonstration of the opportunities for polarization control, we present linear polarization conversion to the orthogonal state. To this end, we appoint asymmetric load values to the four patches. More specifically, we use the complex loads  $\{R_1, C_1\} = \{R_3, C_3\}$  and  $\{R_2, C_2\} = \{R_4, C_4\}$  to electrically emulate the geometric structure of a  $45^\circ$  tilted cut wire, which has been shown in the literature to result in efficient linear polarization conversion [12]. We find that the optimal series  $RC$  values are  $\{R_1, C_1\} = \{R_3, C_3\} = \{0.35 \Omega, 2.6 \text{ pF}\}$  and  $\{R_2, C_2\} = \{R_4, C_4\} = \{3.4 \Omega, 4.8 \text{ pF}\}$  since they allow for the maximum disparity regarding the capacitance values between on- and off-diagonal elements while retaining the total resistance at the lowest possible levels. (Note that for these  $RC$  values, the reactances dominate over the resistances in the neighborhood of 5 GHz.) We succeed in getting perfect polarization conversion to the orthogonal state, i.e.,  $R_{co} = R_{yy} = 0$  at 5.05 GHz, as shown in Fig. 16. However, having used resistance values as high as  $3.4 \Omega$  for the off-diagonal elements, the absorption is high ( $A_y = 61\%$  at 5.05 GHz), limiting the cross-polarized power coefficient to  $R_{\text{cross}} = R_{xy} = 37\%$  [see Fig. 16]. The remaining power is found in transmission (not shown), which is in all

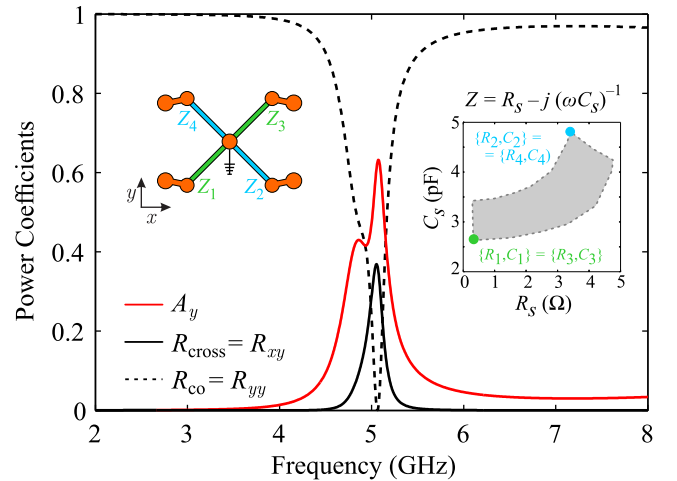


Fig. 16. Linear polarization conversion by electrically breaking the fourfold rotational symmetry using loads  $\{R_1, C_1\} = \{R_3, C_3\} = \{0.35 \Omega, 2.6 \text{ pF}\}$  and  $\{R_2, C_2\} = \{R_4, C_4\} = \{3.4 \Omega, 4.8 \text{ pF}\}$  to emulate a  $45^\circ$  tilted cut wire. Complete polarization conversion to the orthogonal state is observed. The cross-polarized power coefficient is 37% and absorption amounts to 61%. The left and right insets depict the load connectivity and the available  $RC$  range, respectively.

cases small due to the presence of the (perforated) copper backplane. To further quantify the performance, we define the metrics of extinction ( $\text{Ext} = R_{\text{cross}}/R_{\text{co}}$ ) and efficiency ( $\text{Eff} = R_{\text{cross}}/(1 - A)$ ). They describe the completeness of the conversion in reflection and the percentage of cross-polarized reflection out of the power that does not get absorbed. For the case of Fig. 16 their peaks appear at  $\sim 5.05$  GHz and equal  $\text{Ext}_{xy} = 27 \text{ dB}$  and  $\text{Eff}_{xy} = 97\%$ .

Increasing the capacitance  $C_1$  inside the available range, 2.6–3.5 pF, while keeping  $R_1$  constant, we can shift the peak of cross-polarized reflection to lower frequencies. Specifically, the frequency variation can cover a range of 120 MHz. Along this frequency blueshift, we get a decrease in the cross-polarized reflected power since the reactances of the two branches become more comparable; however, the efficiency and extinction remain in all cases very high.

Finally, extending the range of available  $R$  and  $C$  values by the chip to cover lower resistances, reducing the absorption, as well as a wider span of capacitances, to strengthen the reactance dissimilarity between the on- and off-diagonal elements, would further enhance the polarization conversion performance. The extension of  $RC$  range will also enhance the reflected power of anomalous reflection. Alternatively, employing different unit cell topologies, the constraints on the IC range could be relaxed so as to be in line with the practical  $RC$  values available by affordable chip designs.

## IV. CONCLUSION AND FUTURE PROSPECTS

Based on the introduced design procedure and the implementation constraints, we presented a fabrication-ready-tunable microwave metasurface, which offers quasi-continuous local control over the complex surface impedance and allows multiple reconfigurable functionalities. The dynamic control has been achieved by assembling a customized

integrated-circuit chip in each unit cell and codesigning the EM and electronic components to fulfill the desired functionalities. The structure's performance, primarily as a tunable perfect absorber, but also as a tunable anomalous reflector and a polarization converter, has been demonstrated, highlighting the multifunctional character of the proposed reconfigurable metasurface structure. The measured performance of this device will be reported once the ICs have been fabricated, measured, and assembled on the manufactured boards.

HSFs, combining the IC-enabled multifunctional reconfigurable metasurface aspects detailed in this work with appropriate hardware and software, enable themselves to act as hypervisors for metasurface functionalities. In other words, using well-defined application programming interfaces and communication protocols [69], [70], a computer, a software service, or an individual can deploy and chain together multiple EM functionalities over the same HSF. For instance, complex alterations over the phase, amplitude, and polarization can be deployed over an HSF at the same time. Recent studies have also modeled the wavefront detection as a software service, allowing future HSFs to concurrently sense and modify an impinging wave and enabling real-time adaptive operation [71], [72].

The internetworked deployment of multiple HSF units within a space yields a programmable wireless environment (PWE) as a whole, within which EM propagation becomes software-defined [73]. For instance, applying HSF-coatings over walls, ceilings, and other large surfaces in a floorplan, yields an indoors PWE. A central server can orchestrate the EM functionalities deployed to each HSF unit, matching it to the needs of mobile users present in the floorplan. In this manner, studies have showcased novel potential in PWE-assisted channel equalization, multipath fading, Doppler effect mitigation, long-range wireless power transfer, and physical-layer security [74]. These capabilities can enable novel, holistic data networking approaches, which will adaptively and jointly tune the data control logic and the physical propagation characteristics, to optimally serve the user needs.

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**Alexandros Pitilakis** received the Diploma degree in electrical engineering from the Department of Electrical and Computer Engineering, Aristotle University of Thessaloniki (AUTH), Thessaloniki, Greece, in 2005, the M.Sc. degree in electrical engineering from the ENST (Telecom) Paris, Paris, France, in 2007, and the Ph.D. degree from the Department of Electrical and Computer Engineering, AUTH, in 2013.

He was an Intern at the Alcatel-Lucent Optical Transmission Systems Group, Marcoussis, France.

He is currently a Post-Doctoral Researcher with AUTH and the Foundation for Research and Technology Hellas (FORTH), Heraklion, Greece, and teaches undergraduate optics, photonics, and antennas and propagation courses at the University of Western Macedonia, Kozani, Greece. His research interests include computational electromagnetics, waveguides and antennas (optical, terahertz, and RF), metamaterials, nonlinear optics, integrated photonics, plasmonics, and graphene.

Dr. Pitilakis is a member of The Optical Society.



**Anna C. Tasolamprou** received the Diploma and Ph.D. degrees in electrical and computer engineering from the Aristotle University of Thessaloniki (AUTH), Thessaloniki, Greece, in 2006 and 2012, respectively.

She is currently working with the Photonic-Phononic and Meta-Materials (PPM) Group, Institute of Electronic Structure and Laser (IESL), Foundation for Research and Technology Hellas (FORTH), Heraklion, Greece. She has a long experience in analytical and numerical methods for electro-dynamics and an active presence in contemporary applied physics. Her research interests lie in the area of electromagnetics with a focus on the wave propagation properties through random and periodic media, such as photonic crystals, liquid crystals, 2-D materials, metamaterials, and metasurfaces.

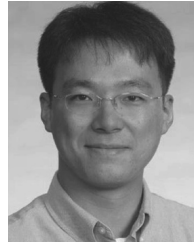


**Odysseas Tsilipakos** (Senior Member, IEEE) received the Diploma and Ph.D. degrees from the Department of Electrical and Computer Engineering, Aristotle University of Thessaloniki (AUTH), Thessaloniki, Greece, in 2008 and 2013, respectively.

From 2014 to 2015, he was a Post-Doctoral Research Fellow with AUTH. Since 2016, he has been a Post-Doctoral Researcher with the Institute of Electronic Structure and Laser (IESL), Foundation for Research and Technology Hellas (FORTH), Heraklion, Greece. His research interests include

metasurfaces and metamaterials, plasmonics and nanophotonics, nonlinear optics in resonant and waveguiding structures, graphene and 2-D photonic materials, and theoretical and computational electromagnetics.

Dr. Tsilipakos is a member of The Optical Society (OSA).

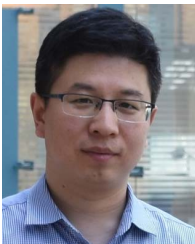


**Do-Hoon Kwon** (Senior Member, IEEE) received the B.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 1994, and the M.S. and Ph.D. degrees in electrical engineering from The Ohio State University, Columbus, OH, USA, in 1995 and 2000, respectively.

He was a Senior Engineer with Samsung Electronics, Suwon, South Korea, from 2000 to 2006. From 2006 to 2008, he was a Post-Doctoral Researcher with the Material Research Science and Engineering

Center and the Department of Electrical Engineering, Pennsylvania State University, University Park, PA, USA. In 2008, he joined the Department of Electrical and Computer Engineering, University of Massachusetts Amherst, Amherst, MA, USA. He was a Summer Faculty Fellow with the Sensors Directorate, Air Force Research Laboratory, Wright-Patterson AFB, OH, in 2011. His current research interests include antenna scattering theory, small/wideband antennas and array elements, frequency-selective surfaces, metamaterials, cloaking, and transformation electromagnetic/optical device designs.

Dr. Kwon was a recipient of the inaugural IEEE Antennas and Propagation Society Edward E. Altshuler Prize Paper Award in 2011.



**Fu Liu** (Member, IEEE) received the B.Sc. degree in applied physics from the China University of Mining and Technology, Xuzhou, China, in 2008, the M.Sc. degree in theoretical physics from Beijing Normal University, Beijing, China, in 2011, and the Ph.D. degree in physics from the City University of Hong Kong, Hong Kong, China, in 2015.

From 2014 to 2016, he was a Research Fellow with the School of Physics and Astronomy, University of Birmingham, Birmingham, U.K. Since 2017, he has been a Post-Doctoral Researcher with the Department of Electronics and Nanoengineering, School of Electrical Engineering,

Aalto University, Espoo, Finland.



**Mohammad Sajjad Mirmoosa** (Member, IEEE) was born in Baft, Iran. He received the Doctor of Science (Technology) degree from Aalto University, Aalto, Finland, in August 2017.

He is currently a Post-Doctoral Researcher with Aalto University. His main research interests include electromagnetic theory, light-matter interaction, and radiative heat transfer.



**Kypros M. Kossifos** (Member, IEEE) was born in Larnaca, Cyprus. He received the Diploma degree in electronic engineering from the ATEI of Athens, Athens, Greece, in 2010, and the M.Sc. degree in electrical engineering from the University of Cyprus, Nicosia, Cyprus, in 2015, where he is currently pursuing the Ph.D. degree.

In 2017, he began working on the FETOPEN project VISORSURF (A Hardware Platform for Software-driven Functional Metasurfaces). His research interests include metamaterials, and

RF/microwave circuits and antennas.



**Dionysios Manassis** received the M.Sc. and Ph.D. degrees in materials science and engineering from the Stevens Institute of Technology, Hoboken, NJ, USA, in 1992 and 1997, respectively, and the project leadership certificate degrees from Cornell University, Ithaca, NY, USA.

He has worked as a Technologist at Universal Instruments Corporation, Conklin, NY. Since 2001, he has been a Senior Technology Scientist with Fraunhofer IZM, Berlin, Germany. His main research interests include fine-pitch flip-chip and wafer-level CSP bumping, solder balling, materials selection for advanced packaging technologies, embedding processes for heterogeneous integration of components in printed circuit boards (PCBs) and optical PCBs, and large-scale prototype manufacturing. In the abovementioned technical fields, he has published extensively in international conferences and peer-reviewed journals.



**Nikolaos V. Kantartzis** (Senior Member, IEEE) received the Diploma and Ph.D. degrees from the School of Electrical and Computer Engineering, Aristotle University of Thessaloniki (AUTH), Thessaloniki, Greece, in 1994 and 1999, respectively.

He is currently a Professor of computational electromagnetics and electromagnetic compatibility with the School of Electrical and Computer Engineering, AUTH. He has authored or coauthored three books, nine book chapters, more than 135 peer-reviewed journal articles, and 230 conference papers. His primary research interests include computational electromagnetics, metamaterials, graphene, real-world EMC/EMI problems, microwaves and antennas, as well as nanotechnology devices.

Dr. Kantartzis is a member of the International Compumag Society (ICS) and the Applied Computational Electromagnetics Society (ACES).



**Christos Liaskos** (Member, IEEE) received the Diploma degree in electrical engineering from the Aristotle University of Thessaloniki (AUTH), Thessaloniki, Greece, in 2004, the M.Sc. degree in medical informatics from the Medical School, AUTH, in 2008, and the Ph.D. degree in computer networking from the Department of Informatics, AUTH, in 2014.

He is currently a Post-Doctoral Researcher with the Foundation for Research and Technology Hellas (FORTH), Heraklion, Greece, where he is handling

the scientific and technical co-ordination task of project VISORSURF. His research interests include computer networks, traffic engineering, and novel control schemes for wireless communications.



**Marco A. Antoniadis** (Senior Member, IEEE) received the B.A.Sc. degree in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 2001, and the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, in 2003 and 2009, respectively.

His research interests include engineered electromagnetic materials (metamaterials and metasurfaces), electrically small antennas, adaptive and reconfigurable antennas, RF/microwave circuits and

devices, implantable/wearable antennas, microwave imaging, wireless power transfer, and radio frequency identification.

Dr. Antoniadis is a member of the IEEE AP-S Education Committee and an Associate Editor of the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION (TAP) and the IEEE ANTENNAS AND WIRELESS PROPAGATION LETTERS (AWPL).



**Julius Georgiou** (Senior Member, IEEE) received the M.Eng. degree in electrical and electronic engineering and the Ph.D. degree from Imperial College London, London, U.K., in 1998 and 2003, respectively.

For two years, he worked as the Head of the Micropower Design in a technology start-up company, Toumaz Technology, U.K. In 2004, he joined Johns Hopkins University, Baltimore, MD, USA, as a Post-Doctoral Fellow. Since 2005, he has been a Faculty Member with the University of Cyprus, Nicosia, Cyprus, where he is currently an Associate Professor.

Dr. Georgiou is a member of the IEEE Circuits and Systems Society (Distinguished Lecturer from 2016 to 2017) and an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and *Frontiers in Neuromorphic Engineering* journal.



**Costas M. Soukoulis** received the Ph.D. degree from the Physics Department, The University of Chicago, Chicago, IL, USA, in 1978.

He is currently a Senior Scientist with the Foundation for Research and Technology Hellas (FORTH), Heraklion, Greece, and a Distinguished Professor of physics with Iowa State University, Ames, IA, USA. His work on photonic bandgaps (PBG), random lasers, plasmonics, graphene, metasurfaces, and nonlinear systems is well known and well received.

He has organized three NATO ASI on PBGs and he was the Director of PECS-VI that took place in Crete in June 2005. He also has five patents concerning the potential applications of the photonic bandgaps and left-handed materials. He recently received the Senior Humboldt Research Award. He has been cited 57 000 times in SCI journals. He has lead research and development projects funded by the EU, NSF, DOE, DARPA, the Office of Naval Research, MUTI-AFOSR, NATO, EPRI, and Ames Lab. He has more than 400 publications in refereed journals and he has given more than 173 invited talks.

Dr. Soukoulis is a fellow of the APS, The Optical Society, and the American Association for the Advancement of Science (AAAS). He was a recipient of the 2014 Max Born Award by the Optical Society of America "for his creative and outstanding theoretical and experimental research in the fields of photonic crystals and left-handed metamaterials." In 2013, he received the McGroddy Prize for New Materials "For the discovery of metamaterials" awarded by the American Physical Society. He was included in the 2014 and 2015 Highly Cited Researchers by Thompson Reuters.



**Maria Kafesaki** received the Ph.D. degree from the Physics Department, University of Crete, Heraklion, Greece, in 1997.

She has worked as Post-Doctoral Researcher with the Consejo Superior de Investigaciones Cientificas, Madrid, Spain, and IESL, FORTH. From 1997 to 2001. She is currently an Associate Professor with the Department of Materials Science and Technology, University of Crete, and an Associate Researcher with the Institute of Electronic Structure and Laser (IESL), Foundation for Research and Technology Hellas (FORTH), Heraklion. She has participated in various European projects as well as in the organization of many international conferences and schools. She has around 130 publications in refereed journals and conference proceedings (with 9200 citations). Her current research is on the area of electromagnetic wave propagation in periodic and random media, with an emphasis on photonic crystals and metamaterials, especially negative refractive index materials.

Dr. Kafesaki is a fellow of the Optical Society of America.



**Sergei A. Tretyakov** (Fellow, IEEE) received the Dipl.Ing.-Physicist, Ph.D., and D.Sc. degrees in radiophysics from Saint Petersburg State Technical University, Saint Petersburg, Russia, in 1980, 1987, and 1995, respectively.

From 1980 to 2000, he was with the Radiophysics Department, Saint Petersburg State Technical University. He is currently a Professor of radio science with the Department of Electronics and Nanoengineering, Aalto University, Espoo, Finland. He has authored or coauthored five research monographs and over 270 journal articles. His current research interests include electromagnetic field theory, complex media electromagnetics, metamaterials, and microwave engineering.

Dr. Tretyakov has served as the General Chair for the International Congress Series on Advanced Electromagnetic Materials in Microwaves and Optics (Metamaterials) from 2007 to 2013, the Chairman for the Saint Petersburg IEEE Electron Devices/Microwave Theory and the Techniques/Antennas and Propagation Chapter from 1995 to 1998, and the President for the Virtual Institute for Artificial Electromagnetic Materials and Metamaterials (Metamorphose VI) from 2007 to 2013.